

**WHAT IS CLAIMED IS:**

1. A semiconductor memory device comprising:

a plurality of memory cells each having a first ferroelectric capacitor for storing data as a polarization value;

5 first voltage applying means for applying a first read voltage between a pair of electrodes of the first ferroelectric capacitor composing the one of the plurality of memory cells from which data is to be read; and

reading means for detecting the polarization value in the first ferroelectric capacitor when the first read voltage is applied between the pair of electrodes of the first ferroelectric capacitor and thereby reading the data stored in the first ferroelectric capacitor therefrom,

a hysteresis loop in the first ferroelectric capacitor is shifted in a direction of voltage opposite in polarity to the first read voltage.

2. The semiconductor memory device of claim 1, wherein the data is complementary data sets and each of the plurality of memory cells has the first ferroelectric capacitors forming a pair to store the complementary data sets.

3. The semiconductor memory device of claim 2, further comprising:

means for writing the same polarization value in each of the first ferroelectric capacitors forming the pair.

20 4. The semiconductor memory device of claim 1, wherein

the data is binary data and each of the plurality of memory cells has, on a one-by-one basis, the first ferroelectric capacitor for storing the binary data, the semiconductor memory device further comprising:

a reference cell having a second ferroelectric capacitor for storing the binary data as a polarization value; and

second voltage applying means for applying a second read voltage between a pair of electrodes of the second ferroelectric capacitor, wherein

the reading means compares the polarization value in the first ferroelectric capacitor when the first read voltage is applied between the pair of electrodes of the first ferroelectric capacitor with the polarization value in the second ferroelectric capacitor when the second read voltage is applied between the pair of electrodes of the second ferroelectric capacitor and reads the binary data stored in the first ferroelectric capacitor therefrom and

a hysteresis loop in the second ferroelectric capacitor is shifted in a direction of voltage opposite in polarity to the second read voltage.

5. The semiconductor memory device of claim 4, wherein the reference cell is composed of a first reference cell having the second ferroelectric capacitor for storing the polarization value corresponding to one of complementary data sets and a second reference cell having the second ferroelectric capacitor for storing the polarization value corresponding to the other of the complementary data sets, the semiconductor memory device further comprising:

means for writing the same polarization value in each of the first and second ferroelectric capacitors.

6. A method for fabricating a semiconductor memory device comprising a plurality of memory cells each having a ferroelectric capacitor for storing data as a polarization value and reading means for applying a read voltage between a pair of electrodes of the ferroelectric capacitor composing the one of the plurality of memory cells from which data is to be read, detecting the polarization value in the ferroelectric capacitor, and thereby reading the data stored in the ferroelectric capacitor therefrom, the method comprising the step of:

applying an AC voltage in which a first voltage having the same polarity as the read voltage is larger in absolute value than a second voltage having a polarity opposite to that of the read voltage to the ferroelectric capacitor a plurality of times.

7. A method for fabricating a semiconductor memory device comprising a plurality of memory cells each having a pair of ferroelectric capacitors for storing complementary data sets as polarization values, voltage applying means for applying a read voltage between a pair of electrodes of each of the pair of ferroelectric capacitors composing the one of the plurality of memory cells from which data is to be read, and reading means for detecting the polarization values in the pair of ferroelectric capacitors when the read voltage is applied between the pair of electrodes of each of the pair of ferroelectric capacitors and thereby reading the complementary data sets stored in the pair of ferroelectric capacitors therefrom, the method comprising the step of:

writing the same polarization value in each of the pair of ferroelectric capacitors and heating the pair of ferroelectric capacitors in each of which the same polarization value has been written to shift a hysteresis loop in each of the pair of ferroelectric capacitors in a direction of voltage opposite in polarity to the read voltage.

8. The method of claim 7, wherein the step of writing the same polarization value in each of the pair of ferroelectric capacitors includes the step of applying a write voltage higher than the voltage applied between the pair of electrodes of the pair of ferroelectric capacitors during a normal operation.

9. The method of claim 7, wherein the step of heating the pair of ferroelectric capacitors is performed at a temperature higher than a temperature reached by each of the pair of ferroelectric capacitors during a normal operation.

10. A method for fabricating a semiconductor memory device comprising a plurality of memory cells each having a first ferroelectric capacitor for storing binary data

as a polarization value, first voltage applying means for applying a first read voltage between a pair of electrodes of the first ferroelectric capacitor composing the one of the plurality of memory cells from which data is to be read, a reference cell having a second ferroelectric capacitor for storing binary data as a polarization value, second voltage  
5 applying means for applying a second read voltage between a pair of electrodes of the second ferroelectric capacitor, and reading means for comparing the polarization value in the first ferroelectric capacitor when the first read voltage is applied between the pair of electrodes of the first ferroelectric capacitor with the polarization value in the second ferroelectric capacitor when the second read voltage is applied between the pair of  
10 electrodes of the second ferroelectric capacitor and reading the binary data stored in the first ferroelectric capacitor therefrom, the method comprising the steps of:

writing the same polarization value in each of the first and second ferroelectric capacitors and heating the first and second ferroelectric capacitors in each of which the same polarization value has been written to shift a hysteresis loop in the first ferroelectric  
15 capacitor in a direction of voltage opposite in polarity to the first read voltage and shift a hysteresis loop in the second ferroelectric capacitor in a direction of voltage opposite in polarity to the second read voltage.

11. The method of claim 10, wherein the step of writing the same polarization in each of the first and second ferroelectric capacitors includes the step of applying a write  
20 voltage higher than each of the voltages applied between the respective pairs of electrodes of the first and second ferroelectric capacitors during a normal operation.

12. The method of claim 10, wherein the step of heating the first and second ferroelectric capacitors is performed at a temperature higher than respective temperatures reached by the first and second ferroelectric capacitors during a normal operation.

25 13. A method for driving a semiconductor memory device comprising a plurality

of memory cells each having a ferroelectric capacitor for storing binary data as a polarization value, voltage applying means for applying a read voltage between a pair of electrodes of the ferroelectric capacitor composing the one of the plurality of memory cells from which data is to be read, and reading means for detecting the polarization value in the ferroelectric capacitor when the read voltage is applied between the pair of electrodes of the ferroelectric capacitor and thereby reading the data stored in the ferroelectric capacitor therefrom, a hysteresis loop in the ferroelectric capacitor being shifted in a direction of voltage opposite in polarity to the read voltage, the method comprising the step of:

applying a write voltage to each of the pair of electrodes of the ferroelectric capacitor such that a first absolute value of the polarization in the ferroelectric capacitor when one of the binary data is stored and a second absolute value of the polarization value in the ferroelectric capacitor when the other of the binary data is stored are different from each other.

14. The method of claim 13, wherein a polarity of the write voltage corresponding to the larger one of the first and second absolute values and a polarity of the read voltage are equal to each other.

15. The method of claim 13, wherein the smaller one of the first and second absolute values is substantially zero.

16. The method of claim 13, wherein a first write voltage with which the polarization in the ferroelectric capacitor has the first absolute value and a second write voltage with which the polarization in the ferroelectric capacitor has the second absolute value are supplied from different voltage sources.

17. The method of claim 13, wherein the read voltage is not more than a coercive voltage of the ferroelectric capacitor.